AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor memory device which has a redundancy circuit comprising:

a plurality of memory blocks; and

a plurality of redundancy memory blocks provided for each of said plurality of memory blocks,

wherein ~~an address bit for selecting each of said plurality of memory blocks is~~ ~~different from an address bit for selecting each of said plurality of redundancy memory blocks~~ each of said plurality of memory blocks includes a plurality of segments,

said plurality of segments are adjacent to one after another,

segments having defects among said plurality of segments are dispersively allocated to said plurality of redundancy memory blocks and replaced by said allocated redundancy memory blocks.

2. (Currently Amended) The semiconductor memory device according to claim 1,

wherein one ~~or more adjacent memory cell rows or columns owned by each of~~ ~~said plurality of memory blocks is a segment which is a unit of allocation as a replacement~~ ~~target, and adjacent segments having defects are replaced by different redundancy memory~~

~~blocks of said plurality of redundancy memory blocks~~each of said plurality of segments includes one or more adjacent memory cell rows or one or more adjacent memory cell columns.

3. (Currently Amended) The semiconductor memory device according to claim ~~2~~1,

wherein ~~address bits that define said segment are lower address bits, and address bits for selecting said plurality of redundancy memory blocks include an address bit immediately above said lower address bits~~a position of an address bit for selecting said plurality of memory blocks is different from a position of an address bit for selecting said plurality of redundancy memory blocks.

4. (Currently Amended) The semiconductor memory device according to claim ~~2~~3,

wherein ~~a unit of said segment is equal to said number of sub-word lines~~address bits that define said plurality of segments are lower address bits, and address bits for selecting said plurality of redundancy memory blocks include an address bit immediately above said lower address bits.

5. (Currently Amended) A semiconductor memory device comprising:

a memory block having a plurality of segments, each of said plurality of segments including a plurality of memory cells; and

a plurality of redundancy memory blocks which are provided for said memory block,

wherein each of said plurality of redundancy memory blocks has a redundancy

segment which substitutes for any segment having a defect among said plurality of segments,

said plurality of segments are ~~cyclically and sequentially~~ allocated to said

plurality of redundancy memory blocks,

a number indicating said redundancy memory block allocated to said any segment

is given by a remainder generated when an address indicating said any segment is divided by a

number of said plurality of redundancy memory blocks, and

each of said plurality of segments is replaceable by said redundancy segment of

said allocated redundancy memory block when having a defect.

6. (Currently Amended) A semiconductor memory device comprising:

a plurality of memory blocks each of which has a plurality of segments, each of

said plurality of segments including a plurality of memory cells; and

a plurality of redundancy memory blocks which are provided for said plurality of

memory blocks,

wherein each of said plurality of redundancy memory blocks has a redundancy

segment which substitutes for any segment having a defect among said plurality of segments,

said plurality of segments are ~~cyclically and sequentially~~ allocated to said

plurality of redundancy memory blocks,

a number indicating said redundancy memory block allocated to said any segment

is given by a remainder generated when an address indicating said any segment is divided by a

number of said plurality of redundancy memory blocks, and

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each of said plurality of segments is replaceable by <u>said redundancy segment of</u> said allocated redundancy memory block when having a defect.

7. (Cancelled)

8. (Currently Amended) The semiconductor memory device according to ~~any one of claims 5 to 7~~<u>claim 5</u>,

wherein a first segment and a second segment of said plurality of segments are adjacent to each other, and a first redundancy memory block allocated to said first segment and a second redundancy memory block allocated to said second segment are different redundancy memory blocks.

9. (Cancelled)

10. (Cancelled)

11. (Currently Amended) The semiconductor memory device according to ~~any one of claims 5 to 10~~<u>claim 5</u>,

wherein each of said plurality of segments is a group of memory cells connected to 2^n (n=0, 1, 2,...) word lines or bit lines, ~~and when a number of said word lines or said bit lines is plural, said word lines or said bit lines are adjacent~~<u>said word lines are adjacent to one after</u>

another when a number of said word lines is plural, and said bit lines are adjacent to one after

another when a number of said bit lines is plural.

12. (Currently Amended) The semiconductor memory device according to ~~any one of~~

~~claims 5 to 11~~claim 5,

wherein a plurality of lower bits of an address inputted to a decode circuit for

selecting any of said plurality of segments are inputted to a decode circuit for selecting said

redundancy memory blocks.

13. (New)   The semiconductor memory device according to claim 6,

wherein a first segment and a second segment of said plurality of segments are

adjacent to each other, and a first redundancy memory block allocated to said first segment and a

second redundancy memory block allocated to said second segment are different redundancy

memory blocks.

14. (New)   The semiconductor memory device according to claim 6,

wherein each of said plurality of segments is a group of memory cells connected

to 2^n (n=0, 1, 2,...) word lines or bit lines, said word lines are adjacent to one after another when

a number of said word lines is plural, and said bit lines are adjacent to one after another when a

number of said bit lines is plural.

15. (New)   The semiconductor memory device according to claim 6,

wherein a plurality of lower bits of an address inputted to a decode circuit for selecting any of said plurality of segments are inputted to a decode circuit for selecting said redundancy memory blocks.